



Verigy Concurrent Test



Complete Concurrent Test Solution

To help bring test costs in line with Moore's Law, Verigy offers a complete testing solution for concurrent test, from design through production. With concurrent test, multiple functional blocks in an SOC can be tested simultaneously, at their native frequencies and voltage levels, dramatically reducing test execution time while boosting tester throughput.

Verigy's concurrent test offering promotes better utilization of valuable testing resources, leading to significantly lower cost-of-test and a better return on investment for valuable tester resources. In fact, as SOC complexity rises, concurrent test becomes more effective because more can be tested in parallel. It is even possible to test multiple Intellectual Property (IP) blocks on multiple devices with Verigy's concurrent test solution, further enhancing tester productivity.

Design Support: EDA tools are a key component to ensure a smooth transition from design to test. Understanding this, Verigy offers design seminars and a design consultancy delivered by a leading EDA company. This allows designers to ensure that their designs can be tested concurrently. In addition, Verigy is working closely with leading EDA companies to create strong links between EDA test

software and the Verigy V93000 SOC Series concurrent test platform. This includes partnering with leaders in the Design-for-Test (DFT) consulting space, since DFT plays a key role in enabling SOC designs to be tested concurrently.

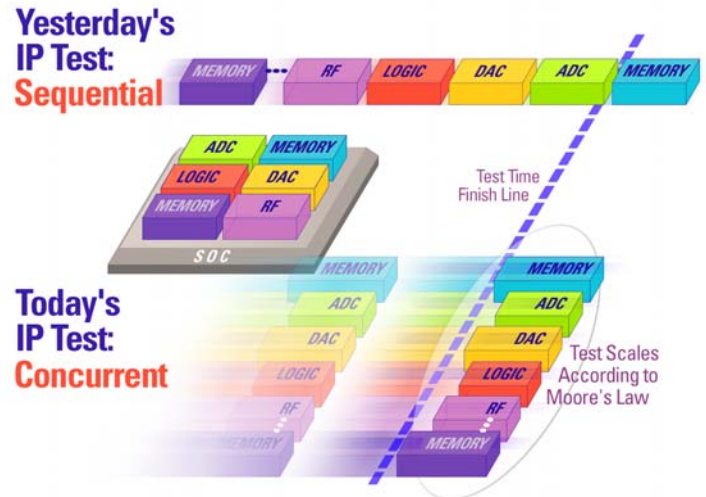
Design to-Test Linkage: To further streamline the transition from design simulation to actual testing, Verigy offers its SmarTest Program Generator (SmarTest PG). This interactive, graphically oriented pattern, timing, and format generation tool helps test engineers create, optimize and debug test programs all in one common environment. SmarTest PG takes design simulation or DFT/ATPG data from the EDA domain and generates test pattern and program files for concurrent test on Verigy's V93000 SOC Series testers.



The V93000 SOC Series Concurrent Test Platform

The enabling technology for Verigy's concurrent test solution is the Verigy V93000 SOC Series test platform – the industry's first multiport ATE architecture designed to support true concurrent test. Essentially, each and every pin in the V93000 SOC Series system provides period, timing, levels, patterns and sequencing, enabling each tester pin to independently operate in any number of different modes. Every pin supports the full range of tester modes including clock, SCAN, BIST-control, functional, APG, and digital source and digital capture.

Having such a flexible arrangement in the V93000 SOC Series testers allows for on-the-fly grouping of pins into a virtual port to test a particular piece of IP. The platform is capable of testing multiple blocks concurrently. Once the test is complete, the tester pins can be immediately reconfigured and assembled into new port configurations to conduct a completely different set of tests.



The v93000 SOC Series features third-generation gigabit digital technology, offering the highest levels of RF, analog and digital integration performance, high accuracy and extremely low noise-floor. Full functionality-test capability in this high-performance platform includes high-speed digital, analog, RF, high-speed buses, serial communications (SerDes), embedded memory and SCAN for maximum manufacturing flexibility.

For more information about Verigy's Concurrent Test, visit our Web site at www.verigy.com/concurrenttest or you can also contact your local test and measurement sales representative. To locate your nearest Verigy office, go to www.verigy.com/find/assist

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June 1, 2006
5988-4429EN

