Yield Learning

Solution Overview

The Yield Learning Solution provides on-tester capture and real-time statistical analysis of electrical failures on complex SOC product die, accelerating time to entitlement yield.

Industry Challenges

One of the biggest challenges in modern nanometer level device design and manufacturing is that "What you see is NOT what you get". The earliest implementation of Design for Manufacturability was the design rule deck. If a designer followed the design rules, yield problems were solved in the fab. Design rule documents in today's sub-micron process technology have exploded to hundred pages of rules and guidelines and they often conflict. Design to process interaction and equipment variations result in significant impact to yield. Now you need to match the design to the fab. Two different products running in the same fab may have vastly different yields, at the same random defect density, simply due to design to fab matching.

Another challenge has been the shift in the economics. Designing for the 65nm or 45nm nodes is expensive. A lot is riding on the time-to-volume-production and time-to-entitlement-yield calculations. It is

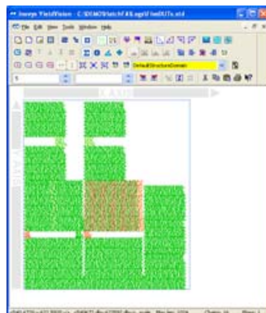
simply too expensive to miss the market window. DFT based yield enhancement methods or logic bit map techniques allow you to look inside the die. Whether it is a systematic defect due to a process weakness or a parametric sensitivity due to a design weakness, most of these problems can be solved either by fab or by the designers. How you chose to solve the problems depends on your access to data and influences the robustness of the final fix.

Product Summary

Get to market on-time and maximize entitlement yield using the most comprehensive product based yield analysis solution in the industry.

The Yield Learning Solution provides on-tester capture and real-time statistical analysis of electrical failures on complex System-on-a-Chip (SOC) product die.

Electrical Fault Map of Die



It efficiently reduces large quantities of electrical failures from probed wafers or packaged parts into specific logical faults. The powerful suite of software analysis and visualization tools enable fast localization of the root cause physical defects, such as: stuck-at defects; timing faults in scan chains and clock trees. The result is significantly faster time to problem diagnosis. The Yield Learning Solution:

- Reduces time and number of wafers to achieve yield entitlement.
- Enables achievement of maximum entitlement yield by eliminating process design interaction yield loss mechanisms
- Increases responsiveness to yield excursions by reducing time to defect detection and diagnosis through a short loop, automated fault localization flow.
- Significantly reduces data log volume by more than 1000x

The Yield Learning Solution consists of three elements:

On-tester Triage: With Triage software, large quantities of electrical failure data are efficiently collected on-tester at the wafer sort stage. Using proprietary algorithms, this data is reduced into a more manageable form showing logical faults.

Analysis and Visualization Tools: The YieldVision analysis and visualization tools show the information in wafer maps, die maps and net maps. The data collected can be stacked and analyzed by die, by wafer, by complete wafer lots, or even across multiple lots by identifying faults with statistical significance:

- Provides prioritization and root cause analysis of the faults which is used to create smart reports. Reports can include histogram data, device hierarchal data, structural data etc.
- Integration around all of these tools into a single tool set – with standard interfaces to existing processes and tools, including fab defect management systems and yield management systems.

Right Test Architecture: The V93000 SOC test system is engineered with the right test architecture, scalable to meet current and future complex SOC/SIP test challenges, and features the industries first on-the-tester fault localization tool.

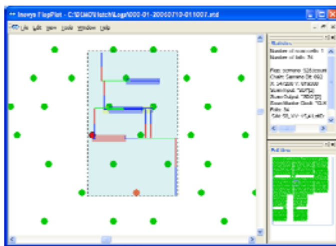
YieldVision

YieldVision provides a layout centric analysis and visualization platform that displays faults and groups of faults in three important views.

Structural View: Faults are displayed showing the faults in a simple row/column format where each row represents a scan chain and each column represents the bit position in that chain. This view provides the analyst with a logic bitmap view of faults in SOC devices, enabling the type of analysis traditionally limited to memory devices.

Hierarchical View: Faults are also displayed showing logic blocks and the design hierarchy. This enables the analyst to focus on specific elements of the design for debug, characterization or yield analysis, enabling parallel efforts on multiple issues without interference.

Physical View: Finally, the faults are displayed showing the physical location of the defect on the die. The physical view includes our unique "splat" level view showing specific net trace paths from the failing observation point. This capability enables fast localization of the root cause physical defects, such as: stuck-at defects; timing faults in scan chains; and clock trees. The result is significantly faster time to problem diagnosis.

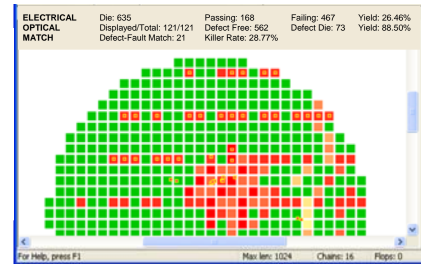


SPLAT showing cone of logic containing fault

Triage

Triage is the pre-analysis module that allows real-time interaction with the tester and fault localization faster than it takes to write the data to disk. Triage performs the necessary on-tester smart data collection and transformation to allow comprehensive analysis and localization of electrical faults.

Electrical/ Optical Defect Overlay Map



End Point Logging: The fundamental principal of Triage is logging the result as opposed to the raw data. Triage logs the chain and bit that captures the result of a failing pattern rather than the raw datalog.

Blocked Chain Faults: Triage uses Fault Targeted Patterns to localize the fault while the die is still in the socket eliminating the time consuming and expensive step of offline simulation. Blocked chain faults can produce millions of failures that can overwhelm traditional approaches leading to long process times and poor hit rates. Now, faster than it takes to log the data to disk, Triage localizes the fault and reports it in a few bytes.

Hold Time Faults: Triage uses Fault Targeted Patterns, generated on-the tester, to localize the fault while the die is still in the socket. Hold time faults are often Vdd sensitive and exhibit a variety of failure signatures. It is not possible to localize the fault based data collected by a production test program. It is necessary to apply additional patterns to localize the faults. Since hold time faults are often design sensitivities, it is important that all of the faults are characterized and reported so that they can all be addressed at one time. Triage performs a comprehensive analysis and reports the faults in a few bytes.

Smart Sampling and Adaptive Data Logging: Yield enhancement is the process of efficiently converting quantity of data into quality of information. Triage provides a smart sampling engine that allows the user to select the right amount of information without modifying the test program. This allows the user to tune the data collection process for first silicon, beginning of the ramp or entitlement yield.

Requirements / Solution Summary Matrix

REQUIREMENTS	SOLUTIONS
Volume yield analysis tools	Multi-wafer or multi-lot analysis tools including trending and visualization tools.
Improvement to tester-centric pin and cycle count format	On-tester conversion to pattern, chain and bit - In the language of the designer - In a design hierarchy context - With accurate x, y die coordinates
Layout extraction	Lightweight net trace from failing flip-flop providing cell and routing level visualization of failures
High-speed, on-tester solution for determining chain faults	On-the-tester adaptive pattern creation for chain failure localization to chain and bit - For blocked chains - For hold-time (Vdd min/max) faults
Adaptive sampling for statistically valid data collection	Automated control of sample rates with smart triggers allow user defined data collection for efficient collection of the data that you need.
Protection for design IP	IP Protected Splats - Client-server type interface to allow communication between the fabless company and the foundry that provides enough information to solve the problem without compromising IP
Link to EDA tools	Import/export solution to EDA tools from Cadence, Mentor Graphics and Synopsys
Ease of use	Award-winning graphical user interface (GUI) that allows any design for test (DFT), failure analysis (FA) or design engineer to say, “I can use it myself!”
Separates visible and non-visible defects	Performs KLARF import and overlay to electrical faults. Performs KLARF export to DMS/YMS tools.
Accuracy, stability, repeatability and reliability, flexibility and scalability	Proven V93000 architecture delivers

Features and Benefits

	FEATURE	BENEFIT
TRIAGE		
Triage	On-the-tester fault localization toolbox	High performance on-the tester analysis and localization of faults running in native Smartest in the Linux environment.
Triage	Blocked Chain Tool	Triage includes our blocked chain tool that localizes blocked chains by running additional patterns on-the-tester.
Triage	Hold Time Tool	Triage includes our hold time tool that localizes hold time faults in chains by running additional patterns on-the-tester.
Triage	Sampling Engine	Our sampling engine allows you to control the data collected using an adaptive datalog control tool.
YIELDVISION		
YieldVision	ATPG link	Minimize data transfer errors with robust bi-directional links to EDA tools.
YieldVision	Complete visualization toolset	Immediately see the failure in Structural, Hierarchical or Physical View. Efficiently map failure to physical defect in Advanced Layout.
YieldVision	Fault analysis and localization	Detect and diagnose elusive new failure mechanisms in smaller geometries – including blocked scan chains and hold-time faults.
YieldVision	Wafer-level debug	Accelerate silicon debug by enabling diagnosis at the wafer level and providing volume data learning.
YieldVision	Single DUT interface board	Faster DUT bring-up time with single interface to design and debug. Use the same interface for production test.
YieldVision	SmartTest operating environment	Classic SmartTest look and feel means that changes to the production environment are minimal.
YieldVision	Leverage V93000 systems	Significantly increase the utilization and performance of installed systems; common platform for engineering and production.
V93000		
Pin Scale	Manage huge ATPG pattern files in production flow	Cycle remapping of failure data to chain/bit is supported in x-modes allowing fault localization in an efficient real-world test program.
Pin Scale	Capture of large amounts of failure data to diagnose faults particularly those on scan chains	Per pin architecture is well suited to collect response data with very little test time overhead. The per-pin architecture only captures the fails on the relevant pins
Pin Scale	Compact data format for volume yield analysis	Conversion to chain and bit information dramatically reduces the volume of data required to document the faults in a production environment
Pin Scale	Pattern-based logging in a format suitable for ATPG tools	Scan structure aware test programs allow pattern-based logging by carrying forward the relevant scan structure information tracking edits and re-mapping the cycles accordingly

Components and Options

- Triage software
- YieldVision software
- V93000 - Works with any Verigy V93000 Pin Scale tester, with PS400, PS800, or PS3600 cards in a compact, small or large test head.

Key Specifications

Import and View Structural test data

- Structural View: by Scan Chain Structure
- Hierarchal View: by Design Architecture
- Physical View: by Physical Layout (wafer or die level)
- Histogram: Sort by Speed

Link to physical layout database

- LEF/DEF interface
- Trace functions (Fan in, fan out)
- Generate IP protected trace picture (i.e. Splat)

Track and Filter by Multiple Fail Variables

- Structural Test: Scan chains, bits in chain, scan patterns, pattern set, etc.
- Manufacturing: program rev, lot ID, wafer ID, facility, XY coordinate, etc.
- Pattern content: execs, bursts, specs, test IDs, etc.

Powerful GUI for Visual Variables

- Zoom to any level of detail within View
- Adjust color thresholds to filter failures by numerical intensity
- Intuitive displays show complete design data on any hierarchy or bit cell

Direct links with Leading ATPG Tools, including:

- Cadence Encounter Test
- Mentor Graphics FastScan
- Synopsis TetraMAX

Linux Based

- Works in conjunction with any Pin Scale V93000
- Available on SmartTest 6.5.2

Interfaces to

- KLARF based inspection tools
- DDMS/YMS

Related information

For more information about Yield Learning, please visit the following website:
www.verigy.com/go/Yield

Contact information

For more information about Yield Learning, please contact your local Verigy sales representative.
www.verigy.com/go/contactus

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