



**Question: “How do I get the expected results when measuring setup and hold time on a DDR interface?”**

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**Question:**

I need to measure setup and hold time on a high-speed DDR interface. When I look at the results the measured setup and hold times are much smaller than expected. What shall I do?

**Answer:**

Please carefully review your measurement setup. High-speed source-synchronous interfaces, like your DDR interface, may show a dynamic behavior where the phase of both clock and data no longer remains constant during transmission of a data pattern. In addition to a static common phase skew between clock and data, a certain common phase drift and/or a common phase jitter may become relevant. Since data and clock are both output with the same clock, the phase variations simply lead to a common phase jitter on both clock and data that does not affect the data transmission. However, during a test on an ATE with fixed timing strobe settings, the common phase jitter or drift causes a data eye to close more than in the real application. It is therefore no longer possible to determine parametric data that are related to the dynamically changing phase of the source-synchronous clock such as a setup or hold time.

In order to ensure accurate testing of high-speed source-synchronous interfaces, the ATE must be able to perform timing related tests relative to the source-synchronous clock, regardless of the static or dynamic properties of the common phase. This can be accomplished by using Verigy's source-synchronous test methodology for testing source-synchronous

interfaces under conditions where the common phase shows dynamic variations in drift and jitter. It allows both measurement (characterization) and validation (pass/fail) of timing parameters with fast throughput as well as detailed analysis of failure mechanisms, e.g. waveform shape, amplitude and spectral content of common phase drift and jitter. With our RSS extension, the data handling and processing can be performed completely in the tester hardware, which enables production-worthy test throughput.